REMARKS

Favorable reconsideration of this application as amended is respectfully requested.

Claim 5 has been cancelled without prejudice or disclaimer. New Claims 12 and 13 have been added to provide specific protection for certain distinctive aspects of Applicants' invention.

Claims 1-4 and 7-11 stand rejected under 35 U.S.C. § 103(a), with independent Claims 1 and 4 rejected as being obvious over Schaefer in view of Clark.

Without acceding to the rejection, Claims 1 and 4 have been amended more particularly to set forth certain distinctive features of Applicants' invention.

As amended, Claim 1 recites that the interface unit includes an external clock output terminal for outputting a clock signal. Claim 1 also recites that the interface unit includes an external data input terminal for inputting external data and a data latch circuit for latching the external data in accordance with the delayed clock signal.

Schaefer fails to teach or suggest the above-mentioned features of Claim 1. For example, the clock signal of Schaefer is a signal provided internally within computer system 100, as will be appreciated from the description of the delay compensation circuit shown in Fig. 2 as "for use

in a DDR memory." See, Schaefer at paragraph 14. The CLKD terminal shown in Fig. 2 of Schaefer is disposed within the delay compensation circuit and merely provides a clock signal to other internal circuit elements. This in contrast to Applicants' invention, which includes an external clock output terminal for outputting a clock signal.

Furthermore, the data output (or DQ) buffers (212a – 212i) of Schaefer are internal circuit elements disposed within the delay compensation circuit for outputting data to other internal circuit elements. In contrast, Applicants' invention includes both an external data input terminal for inputting external data and a data latch circuit for latching the external data in accordance with the delayed clock signal. The output buffers of Schaefer do not correspond to either of these features of Claim 1.

Clark fails to remedy the above-mentioned deficiencies of Schaefer. Accordingly, Claim 1 distinguishes patentably from Clark and Schaefer, and the outstanding rejection of Claim 1 should be withdrawn.

Claim 4 has been amended to recite that the interface unit includes an external clock output terminal, and that the interface unit includes a plurality of external data input terminals for receiving data from the external memory device and a plurality of latch circuits for latching data

received by the plurality of external data input terminals, wherein the latch circuits latch data based on the clock signal as delayed by the load circuit.

As will be appreciated from the above discussion of Claim 1, Schaefer fails to teach or suggest the afore-mentioned features of Claim 4. Nor does Clark remedy these deficiencies. Claim 4 therefore distinguishes patentably from Clark and Schaefer, and the outstanding rejection should also be withdrawn as to Claim 4.

Grossnickle and Strub, which were cited in connection with certain dependent claims, evidently fail to supply the deficiencies of Schaefer and Clark discussed above with respect to independent Claims 1 and 4.

Accordingly, Claims 1 and 4, and their respective dependents, distinguish patentably from the applied references and should now be allowed.

Applicants respectfully request an early Notice of Allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10084) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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